Application No.: 10/099,800 **Docket No.: JCLA8579**

REMARKS

Present Status of Application

The Office Action rejected claims 1-3 and 9-10 under 35 U.S.C.§ 102(e), as being anticipated by Yu (US Patent No. 6,521,502). Claims 1-3 and 6-7 were rejected under 35 U.S.C.§ 102(e), as being anticipated by Park et al. (US Patent No. 6,268,640). Claims 1, 6-7 and 11 were rejected under 35 U.S.C.§ 102(e), as being anticipated by Wong et al. (US Patent No. 6,380,021). Claims 1-3, 6-7, 11-13 and 16 were rejected under 35 U.S.C.§ 103(a) over Applicant's Prior Art (APA) in view of Wong et al.. Claims 4-5 and 14-15 were rejected under 35 U.S.C.§ 103(a) over Applicant's Prior Art (APA) in view of Wong et al., and further in view of Park et al.. Claims 8-10 and 17-19 were rejected under 35 U.S.C.§ 103(a) over Applicant's Prior Art (APA) in view of Wong et al., and further in view of Yu.

The claims 1, 6 and 12 have been amended to provide further descriptions for clarification. This Amendment is promptly filed to place the above-captioned case in condition for allowance. No new matter has been added to the application by the amendments made to the claims, specification or otherwise in the application. After considering the following remarks, a notice of allowance is respectfully solicited.

Discussion for 35 USC 102 & 103 rejections

Claims 1-3 and 9-10 were rejected under 35 U.S.C.§ 102(e), as being anticipated by Yu (US Patent No. 6,521,502). Claims 1-3 and 6-7 were rejected under 35 U.S.C.§ 102(e), as being anticipated by Park et al. (US Patent No. 6,268,640). Claims 1, 6-7 and 11 were rejected under 35 U.S.C.§ 102(e), as being anticipated by Wong et al. (US Patent No. 6,380,021).

Claims 1 and 12 have been amended to provide further description for clarification and define more clearly according to the method of the present invention.

As amended, independent claim 1 recites:

1. A method to suppress a short channel effect of a semiconductor device, comprising:
forming a gate structure on a substrate;
forming a source/drain extension region and a source/drain region in the substrate beside the gate structure;
performing a pocket ion implantation process to form a pocket doped region under the source/drain extension region after forming the source/drain extension region and the source/drain region, and wherein no thermal process is conducted before the formation of the pocket doped region, the source/drain extension region and the source/drain region; and
performing a rapid thermal process to anneal the source/drain extension region, the source/drain region and the pocket doped region concurrently.

(***Emphasis added***)

Applicant respectfully asserts that the amended independent claim 1 patentably distinguishes over the cited references, because the cited references at least lack these features emphasized above (*in bold*).

Yu discloses performing source/drain implant to form source/drain extension 20/22 and performing halo dopant implant to form halo regions 24 before the formation of dielectric spacers 26. In addition, deep source/drain 17/19 is formed after the formation of spacers 26. Obviously, the halo dopant implant is not performed after forming the source/drain extension regions and the

source/drain regions. Therefore, Yu fails to teach or suggest "performing a pocket ion implantation process to form a pocket doped region under the source/drain extension region after forming the source/drain extension region and the source/drain region".

Park teaches forming source/drain extension 6 and halo doping 7 and then performing a thermal annealing step before the formation of spacers 8/9 and the formation of deep source/drain 10.

Similarly, Wong discloses forming NMOS pocket implant 24 and lightly doped N- region 26 and then forming PMOS pocket implants 34. **After** forming PMOS pocket implants 34 and **before** forming lightly doped P- region 36, a rapid thermal annealing is performed. Next, after forming the spacers 40, the source/drain regions 44/46 are formed. Wong clearly teaches forming source/drain regions 44/46 after the formation of the pocket implants 24/34 and lightly doped regions 26/36.

Therefore, neither Park nor Wong discloses "performing a pocket ion implantation process to form a pocket doped region under the source/drain extension region after forming the source/drain extension region and the source/drain region, and wherein no thermal process is conducted before the formation of the pocket doped region, the source/drain extension region and the source/drain region" as claimed in the present invention.

As a result, all these cited references fail to disclose each and every feature of the method as claimed in the present invention.

Claims 1-3, 6-7, 11-13 and 16 were rejected under 35 U.S.C.§ 103(a) over Applicant's Prior Art (APA) in view of Wong et al.. Claims 4-5 and 14-15 were rejected under 35 U.S.C.§

103(a) over Applicant's Prior Art (APA) in view of Wong et al., and further in view of Park et al.. Claims 8-10 and 17-19 were rejected under 35 U.S.C.§ 103(a) over Applicant's Prior Art (APA) in view of Wong et al., and further in view of Yu.

As noted by the Office Action, APA fails to teach a step of performing a rapid thermal process after the formation of the pocket doped region to anneal the source/drain extension region, the source/drain region and the pocket doped region. The Office Action relied on Wong, Park and/or Yu for teaching the lacking features of APA.

Applicant respectfully traverses these rejections for at least the following reasons.

As amended, claim 12 recites:

> 12. A method to suppress a short channel effect of a semiconductor device, comprising:
> forming a gate structure on a substrate;
> performing a first ion implantation process to form a source/drain extension region in the substrate using the gate structure as an implantation mask;
> forming a spacer on a sidewall of the gate structure;
> performing a second ion implantation process to form a source/drain region using the spacer as an implantation mask;
> ***performing a pocket doped implantation process to form a pocket doped region under the source/drain extension region after the formation of the source/drain extension region and the source/drain region, wherein no thermal process is conducted before the formation of the pocket doped region, the source/drain extension region and the source/drain region***; and
> performing a rapid thermal process after the formation of the pocket doped region to anneal the source/drain extension region, the source/drain region and the pocket doped region.

APA clearly discloses performing a first thermal process to anneal the source/drain extension region and the source/drain region. In APA's disclosure, the pocket doped region is formed **after** the first thermal process. Obviously, APA fails to teach "no thermal process is conducted before the formation of the pocket doped region, the source/drain extension region and the source/drain region", because APA suggests performing a thermal process before the formation of the pocket doped regions.

Neither Wong, Park nor Yu remedy deficiencies of APA, either in combination or alone, because none of the references teach or suggest "no thermal process is conducted before the formation of the pocket doped region, the source/drain extension region and the source/drain region" for the method of this invention.

As discussed above, the Park reference and the Wong reference teach performing a thermal annealing process before forming the source/drain regions, while APA teaches performing a thermal process before the formation of the pocket doped regions. None of the cited references recognize the advantages of the present invention or the importance of not performing a thermal process before the formation of the source/drain extension region, the source/drain region and the pocket doped region.

On the contrary, the present invention teaches conducting a thermal process to anneal the source/drain extension region, the source/drain region and the pocket doped region after the formation of the source/drain extension region, the source/drain region and the pocket doped region. Since the thermal process is not performed after the formation of the source/drain extension region and the source/drain region, the dopants in the pocket doped region are then trapped in the lattice defects from implantation to reduce the diffusion of the dopants in the pocket doped region during the subsequent thermal process.

As a result, Applicant submits that amended independent claims 1 and 12 patently define over the cited references. For at least the foregoing reasons, all pending claims patently define over the cited references and should be allowed. Accordingly, the rejection under § 102 and 103 should be withdrawn.

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CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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